CLAIMS:

1. A multiprocessor array which includes

a) a first processor shadow register unit (1) which operates within a first clock domain and includes

i) a first processor (2), and

ii) a first shadow register unit (3) which is connected to the first processor (2) so as to transmit data,

b) at least one second processor shadow register unit (9) which

i) operates within a corresponding second clock domain,

ii) includes a second processor (10), and

iii) a second shadow register unit (11) which is connected to the second processor (10) so as to transmit data, and

c) a peripheral unit (17) which operates within a peripheral clock domain and includes

i) a multiplexer unit (18) which is connected to the first shadow register unit (3) and the at least one second shadow register unit (11) so as to transmit data,

ii) a register unit (20), the construction of the first shadow register unit (3) and the at least one second shadow register unit (11) and the register unit (20) being identical in respect of function, and

iii) a priority unit (19) for allocating the multiplexer unit (18) for data transmission to the first shadow register unit (3) or to the at least one second shadow register unit (11), the priority unit (19) being connected so as to transmit data to the first shadow register unit (3) and to the at least one second shadow register unit (11).

2. A multiprocessor array as claimed in claim 1, characterized in that the first shadow register unit (3), the at least one second shadow register unit (11) and the register unit (20) include status flags as well as control/data registers.

3. A multiprocessor array as claimed in claim 1 or 2, characterized in that the first clock domain and/or the at least one second clock domain include more than one processor.

4. A multiprocessor array as claimed in one of the preceding claims, characterized in that in order to read out data from the first shadow register unit (3) and/or the at least one second shadow register unit (11) the multiplexer unit (18) is connected thereto in the read out direction.

5. A multiprocessor array as claimed in one of the preceding claims, characterized in that requests for access from the first shadow register unit (3) and/or the at least one second shadow register unit (11) to the priority unit (19) are encoded as a one-bit signal.

6. A multiprocessor array as claimed in one of the preceding claims, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: first-come, first-served.

7. A multiprocessor array as claimed in one of the claims 1 to 5, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: all shadow register units (3, 11) are served successively.

8. A multiprocessor array as claimed in one of the claims 1 to 5, characterized in that the priority unit (19) grants priority to the first shadow register unit (3) or to the at least one second shadow register unit (11) in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit (17).

9. A multiprocessor array as claimed in one of the preceding claims, characterized in that the peripheral unit (17) is constructed as an infrared interface, UART interface or USB interface.

10. A multiprocessor array as claimed in one of the preceding claims, characterized in that the first shadow register unit (3) and/or the at least one second shadow register unit (11) are connected to the associated processor (2, 10) via an interrupt (8, 16).

11. A communication terminal using a multiprocessor array as claimed in the preceding claims.

12. A portable device using a multiprocessor array as claimed in the preceding claims.